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EXAMINER	
HASSAN, AURANGZEB	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/699,473	Applicant(s) HAN, JONGHEE	
	Examiner Aurangzeb Hassan	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 10 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The newly amended claim limitations necessitate a round-trip path that **does not include** the receiver/receiving circuit. The specification and a round-trip path in paragraphs 34 and 35 as being a signal that is transmitted from a controller to a receiver and a buffer in turn transmits a return signal back to the controller. Without the receiver the initial strobe clock signal would not be substantiated as seen in figures 3 and 4. Accordingly the Examiner will best interpret the claims to represent a round-trip path as best enabled by the specification (paragraphs [0034 & 0035]).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 16, 18, 27, 29, 32 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The newly amended claim limitations necessitate "**a portion**" of the first signal path forming part of the round-trip path. It is unclear what is represented by "**a portion**" and therefore the metes and bounds of the "round-trip path" is unclear and will be best interpreted by the examiner to represent the round-trip path having a **dependency upon** the first signal path.

Appropriate clarification/correction required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 5 – 14, 16 – 21, 23, 26 – 30, 32, 34 – 40 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Leahy et al (US Patent Number 5,029,124, hereinafter "Leahy").

7. As per claim 1, Leahy teaches a method comprising:

driving first data on a data bus (data 34 on data bus 14, figure 2);

transmitting, via a first signal path (38, figure 2), a strobe signal to a receiving circuit (receiving circuit 12, figure 2) indicating the validity of the first data on the data bus (first signal line DATA VALID, column 5, lines 44 – 53);

receiving a return signal in the form of the strobe signal transmitted via a second signal path (40, figure 2), wherein the second signal path and a portion of the first signal path form a round-trip path having a propagation delay such that the arrival of the return signal indicates an assumed arrival of the strobe signal at the receiving circuit (DATA VALID and ACKNOWLEDGE signals, column 1, lines 24 – 59); and

in response to receiving the return signal, driving second data on the data bus (in synchronous data transmission the second data is driven over the bus).

8. As per claims 2 and 23, Leahy teaches a method wherein driving the first data and the second data on the data bus comprises enabling a driver to drive the data (asserting DATA VALID control signal along interface bus from source via sequencer 70, figure 3).

9. As per claims 5 and 6, Leahy teaches a method wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (column 2, lines 9 – 32).

10. As per claim 7, Leahy teaches a method wherein the return signal is the strobe signal (ACKNOWLEDGE strobe signals along 40, figure 2).

11. As per claim 8, Leahy teaches a method further comprising generating the return signal by the receiving circuit (ACKNOWLEDGE strobe signals along 40, figure 2).

12. As per claim 9, Leahy teaches a method wherein generating the return signal comprises buffering the strobe signal (synchronizing signal buffer, column 9, lines 22 – 25).

13. As per claim 10 Leahy teaches a method comprising,

driving a first data on a data bus (data 34 on data bus 14, figure 2);

issuing a strobe signal from a controller (DATA VALID 38 , figure 2);

receiving, by a receiving circuit (receiver 12, figure 2), the strobe signal a period of time after issuing the strobe signal; in response to receiving the strobe signal by the receiving circuit, latching in the first data from the data bus (latching upon DATA VALID);

receiving, by the controller, the strobe signal a period of time after issuing the strobe signal, wherein the controller receives the strobe signal via a round-trip path (ACKNOWLEDGE 40, figure 2); and

in response to receiving the strobe signal by the controller, driving a second data on the data bus (de-asserts strobes and drives next data word on bus).

14. As per claim 11, Leahy teaches a method wherein (a)-(f) are performed bidirectionally over the data bus (bidirectional line 34, figure 2).

15. As per claims 12, 17 and 25 Leahy teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein only a portion of each path shares a common line (first path 38 and second path 40, figure 2, round-trip data valid to acknowledge).

16. As per claim 13, Leahy teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein lengths of the first and second paths are substantially the same (figure 2, signal lines 38 and 40).

17. As per claim 14, Leahy teaches a method comprising, latching the second data in from the data bus (second data is latched upon reception of second DATA VALID via 34 and 38, figure 2).

18. As per claims 16, 18, 27 and 29, Leahy teaches a method comprising, by a driver controller (10, figure 2):

driving first data on a data bus (34, figure 2);

(As per claim 18, driving by a driver which asserts DATA VALID control signal along interface bus from source via sequencer 70, figure 3)

transmitting a data strobe signal to a receiver via a forward signal path (strobe on 38, figure 2, as per claim 18, transmits when data is ready);

receiving the data strobe signal via a return signal path, wherein a portion of the forward signal path and the return signal path form a round-trip signal path that does not include the receiver and receipt of the strobe signal indicates an assumed arrival of the strobe signal at the receiving circuit via the forward signal path (receive strobe on 38, figure 2 and transmit return on 40, figure 2); and

in response to receiving the strobe signal, driving second data on the data bus (next data word transmitted after acknowledge signal de-asserted, column 7, lines 50 – 62); and

by a receiver: receiving the strobe signal via the forward signal path (receives data valid signal on 38, figure 2); and

in response to receiving the strobe signal, latching the fist data in from the data bus (clock in data upon arrival of data valid signal, column 6, lines 28-39).

19. As per claims 19 and 20, Leahy teaches a method wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (column 2, lines 9 – 32).

20. As per claim 21, Leahy teaches a method wherein receiving the strobe signal by the control circuit occurs substantially simultaneously with receipt of the strobe signal by the receiving circuit (asynchronous protocol, figure 5).

21. As per claim 26, Leahy teaches a method, wherein the first line is couple to the receiving circuit (figure 2).

22. As per claim 28, Leahy teaches a device wherein the round-trip path is partially defined by the strobe clock signal line (internal clock basis of strobes, column 11, lines 44 – 47).

23. As per claim 32, Leahy teaches a circuit comprising:

a controller (10, figure 2) comprising a strobe clock signal output (38, figure 2) and a return clock signal input (40, figure 2) and configured to issue a first enable signal (DATA VALID) and a second enable signal (second DATA VALID iteration asserted), the first enable signal enabling a plurality of drivers to drive respective first data on respective data lines, and the second enable signal enabling the plurality of drivers to drive respective second data on their respective data lines (column 4, lines 24 – 41).;

a strobe clock signal line coupled to the strobe clock signal output (DATA VALID on internal clock basis of strobes, column 11, lines 44 – 47); and

a return clock signal line coupled to the return clock signal input; wherein a portion of the strobe clock signal line defines an initial portion of a path and the return clock signal line defines a terminal portion of the round-trip path (AVAILABLE signal line is directly dependent on the DATA VALID thus the initial portion to complete the round-trip); and wherein the controller is configured to;

respond to an external clock signal by pulling a strobe clock signal to a first state on the strobe clock signal line and pulling the first enable signal to an active state (asserting the DATA VALID when ready for words, based upon appropriate timing of clock, column 6, lines 8 – 15);

receive a return clock signal on the return clock signal line a period of time after pulling the strobe clock signal to the first state, wherein the return clock signal is timed off of the strobe clock signal and indicates an assumed receipt of the strobe clock signal in the active state by receiving circuitry coupled to the respective data lines and configured to latch in the first and second data from the data lines in response to the strobe clock signal (burst mode synchronization of data latching by 10 and 12, column 6, lines 28 – 39); and

respond to the received return clock signal by pulling the second enable signal to an active state (next word clocked on burst, 38 – 48).

24. As per claim 34, Leahy teaches a circuit wherein the strobe clock signal is coupled to the return clock signal line and to the receiving circuitry (DATA VALID and

ACKNOWLEDGE are coupled as they are codependent and coupled to receiver 12, figure 2, column 5, lines 54 – column 6, line 2).

25. As per claim 35, Leahy teaches a circuit wherein the receiving circuitry is configured to latch in the first data from the data lines in response to receiving the strobe clock signal in the first state (on first iteration of DATA VALID on 38, receiver 12 will latch onto the data words on data bus 34, figure 2) and to latch in the second data from the data lines in response to receiving a transition of the strobe clock signal from the first state to a second state (once AVAILABLE signal is de-asserted the second iteration of DATA VALID proceeds to re-assert for second iteration of data).

26. As per claims 36 and 38, Leahy teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (both clock based signals, AVAILABLE is a delayed instance of DATA VALID).

27. As per claim 37, Park teaches a circuit wherein the strobe clock signal and the return clock signal are issued within a single period of an external clock signal (asynchronous protocol, figure 5).

28. As per claim 39 Leahy teaches a device comprising,

a bidirectional data bus (element 34, figure 2);

a first driver circuit coupled to the bus and configured to propagate a first data and a second data in a first direction along the bus (asserting DATA VALID control signal along interface bus from source via sequencer 70, figure 3);

a first receiver circuit coupled to an end of the bus opposite the first driver circuit and configured to latch the first and second data in response to a first strobe clock signal (transceivers 96, figure 4);

a second driver circuit coupled to the bus and configured to propagate a third data and a fourth data in a second direction along the bus (asserting DATA VALID control signal along interface bus from source via sequencer 60, figure 3);

a second receiver circuit coupled to an end of the bus opposite the second driver circuit and configured to latch (transceivers 98, figure 4);

a first controller configured to enable the first driver circuit and to generate the first strobe clock signal (first Enable/assertion of DATA VALID, SYCH IN 38, figure 2);

a second controller configured to enable the second driver circuit and to generate the second strobe clock signal (second iteration Enable/assertion of DATA VALID, SYCH IN 38, figure 2);

a first strobe clock signal line to propagate the first strobe clock signal from the first controller to the first receiver circuit (internal clock basis of strobes, column 11, lines 44 – 47);

a first round-trip path comprising a first return path for the first strobe clock signal back to the first controller (38 and 40, figure 2);

a second strobe clock signal line (internal clock basis of strobes, column 11, lines 44 – 47) to propagate the second strobe clock signal from the second controller to the second receiver circuit; and

a second round-trip path comprising a portion of the second strobe clock signal line and a second return path for the second strobe clock signal back to the second controller (DATA VALID and ACKNOWLEDGE strobe signals transmitted along data bus 14, figure 2, second data is transmitted after acknowledgement sent, column 1, lines 24 – 59, with each iteration the strobe signals are toggled allowing for the second round-trip path).

29. As per claim 40, Park teaches a device wherein the first round-trip path is partially defined by the first strobe clock signal line and the second round-trip path is partially defined by the second strobe clock signal line (internal clock basis of strobes, column 11, lines 44 – 47, first path 38 and second path 40, figure 2, round-trip data valid to acknowledge).

30. As per claim 42, Park teaches a device wherein the first strobe clock signal line comprises at least a portion of the second strobe clock signal line (internal clock basis of strobes, column 11, lines 44 – 47, first path 38 and second path 40, figure 2, round-trip data valid to acknowledge).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claims 3, 4, 15, 22, 24, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leahy in view of Park (US Patent Number 6,147,926).

33. As per claims 3, 22 and 33, Leahy teaches a method wherein the data bus is internal to memory comprising devices in a system (dual port RAM for FIFO register mean, figure 3 and 4, column 13, lines 31 – 40).

Park teaches a method wherein the data bus is an internal data bus of the multiple data rate memory device (column 4, lines 1 – 20).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Park with the well-known handshaking of Leahy. One of ordinary skill would be motivated to make such modifications in order to reduce latency in the transfer of a large amount of data in a data processing system (column 2, lines 50 – 57).

34. Leahy as modified by the teachings of Park as applied to claim 3 above, as per claims 4, 15, 24 and 31, Park teaches a method wherein the multiple data rate memory

device is a double data rate synchronous dynamic random access memory (DDR SDRAM) (DDR SDRAM, column 4, lines 14 – 16).

Response to Arguments

35. Applicant's arguments with respect to claims 1 – 40 and 42 have been considered but are moot in view of the new ground(s) of rejection which have been best interpreted as shown above in the 112 1st and 2nd paragraph rejections.

Conclusion

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER
9/11/07